REMARKS/ARGUMENTS

Prior to this amendment, claims 1-15 and 17-22 were pending. In this amendment, claims 1-2, 4, 7, 9-13, and 17-22 are amended. Thus after entry of this amendment, claims 1-15 and 17-22 will remain pending.

Allowable Subject Matter

Applicants note with appreciation the indicated allowability of claims 2-11.

Rejection under 35 USC § 112, indefiniteness

Claims 17-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claim 17 and 20, the term "form" is asserted to be ambiguous. The term "form" has been removed. Accordingly, Applicants request withdrawal of this rejection.

As to claims 18 and 21, the use of the term "only if" in conjunction with the term "only if" in the parent claims is asserted to be unclear. The term "only" has been removed from these claims as well as the parent claims. Accordingly, Applicants request withdrawal of this rejection. Furthermore, the restriction to only one necessary condition is achieved by the term "if and only if" and not by the term "only if." Thus, two "only if" statements (i.e. two necessary conditions) is logically possible.

As to claims 19 and 22, the term "relates" is asserted as being ambiguous. The term "relates" has been removed. Accordingly, Applicants request withdrawal of this rejection.

Rejection under 35 USC § 102, Azevedo et al.

Claims 1 and 12-15 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Azevedo et al. (US Patent Number 7,035,979).

Claims 1-11

Claim 1 is allowable as Azevedo does not teach or suggest each and every element of claim 1. For example, claim 1 recites:

> *testing whether a present read access request is such that there is a high probability that said present read access request relates to configuration data for said programmable logic device; and*
>
> *performing a prefetch operation if it is determined that there is a high probability that said present read access request relates to configuration data for said programmable logic device.*

Azevedo anticipates future data requests sent from a processor 710 to a memory 780 by using pattern recognition. *See Azevedo*, col. 11 lines 41-44, FIG. 7, and col. 9 lines 49-52. Once a pattern of data requests is recognized, upcoming cache lines that are part of the recognized pattern are prefetched. *Id.*, col. 12 lines 4-7. The data in a particular cache line is prefetched when a request for that data usually follows the data of a previous request. *Id.*, col. 12 lines 7-10. Thus, prefetching of a particular cache line is not done based on the type of data, such as configuration data for a programmable logic device, but on the ordering of data requests, regardless of type. *Id.*, FIG. 10.

Configuration data is a particular type of data and is a common term known in the field of programmable logic devices. "The logic elements ..., their interconnections, and the connections between the logic elements and the input/output devices 106,108, are all programmable, on the basis of configuration data, so that the programmable logic device 100 performs a specific intended function." *See present specification*, page 4 lines 10-13. Azevedo does not mention data being used to configure logic elements and interconnections, and as such does not teach or suggest testing whether a read access request is related to configuration data for a programmable logic device, as recited in claim 1.

Additionally, Azevedo does not mention a programmable logic device. "A programmable logic device ... is made up of a large number of programmable logic elements" that may be configured to perform different functions. *See present specification*, page 4 lines 8-13. As is common in the art of processors, a processor 710 and the caching assistant processor core 740 perform predetermined functions in an order specified by program code. *See Azevedo*,

FIG. 7 and col. 9 lines 58-66. Thus, neither processor 710 nor the caching assistant processor core 740 are programmable logic devices as the functions of the instruction set for the processors are fixed. Accordingly, Azevedo does not teach or suggest performing a prefetch if there is a high probability that the data request "*relates to configuration data for said programmable logic device*," as recited in claim 1. Furthermore, even if the caching assistant were programmable, it does not use and is not configured by the data from memory 780, but passes the data to the processor 710. *Id.*, col. 10 lines 14-18 and FIG. 7.

For at least the reasons stated above, Applicant submits that claim 1 and its dependent claims 2-11 are allowable over the cited references.

Claims 12-15 and 17-22

Applicants submit that independent claims 12 and 13 should be allowable for at least the same reasons as claim1. Claims 17-19 depend from claim 12, and claims 20-22 depend from claim 13 and thus derive patentability at least therefrom.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

David B. Raczkowski
Reg. No. 52,145

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 415-576-0200
Fax: 415-576-0300
DBR:lrj
60980834 v1